

## **AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

### **Listing of Claims:**

1           1. (Currently amended) A packet buffer control system comprising:  
2           a memory storing bytes of data in lines;  
3           a packet buffer, the packet buffer divided into a first section and a second  
4 section, each section for storing bytes of data in lines; and  
5           a packet buffer controller that receives a line of data from said memory  
6 along with a tag indicating a shift value and shifting said received line of data in  
7 accordance with the shift value for storage in said first section and in said second  
8 | section, wherein storage in said first section and in said second section occur  
9 | simultaneously.

1           2. (Original) The packet buffer control system of claim 1 wherein said  
2 packet buffer controller comprises a wrap-around shift register in which said  
3 received line of data is shifted for storage.

1           3. (Original) The packet buffer control system of claim 1 further  
2 comprising means for masking a line in said packet buffer.

1           4. (Original) The packet buffer control system of claim 1 wherein storage  
2 of a line of data in the first section and in the second section is accomplished in a  
3 single clock cycle.

1           5. (Original) The packet buffer control system of claim 1 wherein the  
2 packet buffer controller further includes logic that reads a first output data line  
3 from the first section and then reads a second output data line from the second  
4 section for transmission to a network.

1           6. (Currently amended) A method of communicating alignment  
2 information comprising:  
3           preparing read requests for lines of data to fill a packet payload;  
4           obtaining a shift value corresponding to any misalignment between the  
5 lines of data and the packet payload;  
6           sending a read request including a tag with the shift value, said tag being  
7 for inclusion in a response to the read request;  
8           receiving at a packet buffer controller the response having a line of data  
9 and the tag; and  
10          shifting the line of data in accordance with the shift value in the tag and  
11 writing the shifted line of data into a first section and a second section of the  
12 packet buffer, wherein writing the shifted line of data into said first section and  
13 said second section occur simultaneously.

1           7. (Original) The method of claim 6 wherein writing the shifted line of  
2 data is accomplished in a single clock cycle.

1           8. (Original) The method of claim 6 wherein said act of writing writes  
2 bytes of the shifted line of data that are in unmasked positions of the packet buffer  
3 into the packet buffer while bytes of the shifted line of data in masked positions of  
4 the packet buffer do not make changes to the masked positions of the packet  
5 buffer.

- 1           9. (Original) The method of claim 6 further including:
- 2           reading a first output data line from said first section and then reading a
- 3           second output data line from said second section for transmission to a network.